Final Report

Study on the hydrogenated ZnO-based thin film transistors

To

Dr. Gregg Jessen

Asian Office of Aerospace Research & Development

April 30th, 2011

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Report Documentation Page

Form Approved
OMB No. 0704-0188

1. REPORT DATE	2. REPORT TYPE	3. DATES COVERED
19 AUG 2011		

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Study on the hydrogenated ZnO-based thin film transistors ? Part I	5b. GRANT NUMBER
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S)	5d. PROJECT NUMBER
Jae Hyung Jang	5e. TASK NUMBER
	5f. WORK UNIT NUMBER
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
Gwangju Institute of Science and Technology,1 Oryongdong Bukgu,Gwangju 500-712,South Korea,NA,NA	**N/A**
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
	11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

In Part I of this project, attempts to develop low capacitance, depletion-mode ZnO-based thin-film transistors (TFTs) were studied using two approaches. The first approach used elevated substrate temperature growth of a-IGZO channel layers, but most of the devices exhibited enhancement-mode operation. The second approach studied the effect of hydrogenation of a-IGZO channel layers during post-annealing. Even though the device quality improved, depletion-mode operation was not achieved. Depletion-mode operation was achieved in Part II of this project to be reported separately.

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			
unclassified	**unclassified**	**unclassified**		**16**	

Contents

Summary

In this research activities on the development of ZnO-based thin film transistors (TFTs) for the THz switching devices, we had three technical approaches to achieve the depletion-mode devices with very low capacitance.

The first approach studied the effect of the substrate temperature during the deposition of a-IGZO channel layer. By elevating the substrate temperature from room temperature to 200oC, the device performance could be improved in terms of field effect mobility and saturation current level, but most of the devices exhibited enhancement-mode operational characteristics.

For the second approach, we have investigated the hydrogenation of a-IGZO channel layer during the post-annealing process. The saturation current level and the field effect mobility of the devices dramatically improved when they are compared with those of the devices annealed under nitrogen ambiance. Even though they exhibited order of magnitude higher field effect mobilities, the carrier concentration did not increase a lot so that the threshold voltage of the devices still exhibited positive values, which is not proper for the THz switch application.

From these two experiments, the post-annealing process under nitrogen ambiance and over pressure hydrogen ambiance, could improve the interface between the channel layer and the gate dielectric, and the quality of the channel layer. It leaded to the improved field effect mobility and the saturation current level. But they did not increase the carrier concentration, which can be seen from the threshold voltage shifts. All the devices with the current a-IGZO film seems to have less carrier concentration to achieve depletion-mode devices. From these observation, we should use different composition in a-IGZO film to increase the carrier concentration in the channel. This study will be carried out in the next year.

Chapter 1.

The effect of substrate temperature during the deposition of a-IGZO film on the performance of thin film transistors

Introduction

The effect of substrate temperature during depositing IGZO channel layer on the performance of amorphous indium-gallium-zinc oxide (a-IGZO) thin film transistors (TFTs) was investigated. The most critical temperature during the processing of IGZO TFT is known to be the post-annealing temperature because the post-annealing temperature is generally higher than the deposition temperature. However, the initial channel deposition temperature can also affect the quality of interface between the gate dielectric layer and the IGZO channel layer. In this study, we have investigated the performance of the devices deposited at room temperature (RT) and 200^{o}C followed by post-annealing at 300, 305, and 310^{o}C.

Fabrication details of bottom-gated a-IGZO TFTs

The fabrication process began with Corning 1737 glass substrates coated with 200-nm-thick indium tin oxide (ITO) (sheet resistance =4~8 Ω/□, Delta Technologies limited, USA). The ITO layer was patterned using photolithography and LCE-12k (ITO etchant, Cyantek Corporation) wet etchant at 33^{o}C for 10min to define bottom gate electrodes. The 50-nm-thick silicon nitride gate insulator was deposited by plasma enhanced vapor deposition system utilizing SiH_4, NH_3, N_2, and He gases at 300^{o}C. After the deposition of silicon nitride, 50-nm-thick undoped IGZO film was grown by rf magnetron sputtering system with facing target configuration. The IGZO sputtering conditions were a pure Ar (8sccm), an rf power of 350 W, working pressure of 5 mTorr, and deposition temperature of room temperature. The deposited IGZO film was subsequently patterned by photolithography and a

wet etching by diluted HCl (300:1). Silicon nitride gate dielectric was etched by inductively coupled plasma etcher system using SF_6/O_2 gas mixtures to form via holes for contact to ITO gate electrodes. Finally, Multilayer Ti/Pt/Au metallization was e-beam evaporated and lifted-off for source and drain contacts.

After the fabrication, the TFTs were annealed in an N_2 ambient at various temperatures (300, 305, and 310^{o}C) for 35min.

The electrical characteristics of fabricated TFTs having a channel width (W) of 200 μm and a length (L) of 5 μm were measured using a semiconductor parameter analyzer (HP-4155A).

Results

The as-fabricated TFTs using IGZO channel layer deposited on an unheated substrate exhibited drain currents of only around 0.1μA at V_{GS}=25. The as-deposited TFTs with IGZO grown on an unheated substrate showed the field-effect electron mobility of 0.001 cm^2/Vs, threshold voltage of 7.4 V, subthreshold voltage swing of 4.60 V/decade, and the on/off current ratio of 1.0×10^4.

The as-fabricated TFTs using IGZO channel layer deposited on a heated substrate (200^{o}C) exhibited the field effect mobility of 0.05 cm^2/V s, on/off current ratio of 10^5, the threshold voltage of 3.1 V and the subthreshold voltage swing of 4.48 V/decade.

Even though The HT-TFTs exhibited the better performance than the RT-TFTs, the performance of the TFTs should be further improved. For the further performance enhancement, post-annealing process at temperatures of 300, 305, and 310^{o}C were carried out for the RT-TFTs and HT-TFTs under N_2-ambiance.

The transfer characteristics of the RT-TFTs and HT-TFTs processed under various post-annealing condition are shown in Fig.1.1 and Fig.1.2, respectively. The transfer characteristics of the devices were measured at V_{DS}=20 V. As-fabriated RT-TFTs exhibit very poor characteristics but their performance improves drastically after annealing at temperatures of 300, 305, and 310^{o}C.. As the

annealing temperature changes from 300^{o}C to 310^{o}C, the RT-TFTs exhibited negative shift in threshold voltage, the better subthreshold voltage swing and the higher field effect mobility. The best electrical performance of RT-TFTs was obtained from the devices annealed at 310^{o}C for 35min; field effect mobility of 11 cm^{2}/Vs and subthreshold voltage swing of 0.73 V/decade.

HT-TFTs show similar trends with RT-TFTs in terms of the performance variation with respect to the annealing temperature. Post-annealing leads to performance improvement of the devices. As compared with the RT-TFTs, the HT-TFTs demonstrated the higher field effect mobility after annealing at all temperatures of 300, 305, and 310^{o}C. The best field effect mobility of HT-TFTs was 17 cm^{2}/Vs which was higher than that of RT-TFTs (11 cm^{2}/Vs). Threshold voltage of HT TFTs was shifted from 3.1 V to -0.1 V after post-annealing for the devices annealed at 310^{o}C.

Figures 1.3 and 1.4 show the output characteristics of both as-fabricated RT TFTs and HT-TFTs, respectively. The saturation current of as-fabricated HT-TFTs was 1.1μA under a gate bias of 20 V. The current level was higher than that of as-fabricated RT-TFTs. Figures 1.5 and 1.6 show the output characteristics of both RT-TFTs and HT-TFTs annealed at 310^{o}C for 35min. As shown in the figures, the post-annealing process effectively elevates the saturation current level as compared to that of as-fabricated devices.

Conclusion

This study investigated that the deposition temperature of an IGZO channel layer can influence the electrical performance of IGZO TFTs. When both the TFTs with IGZO film deposited at 200^{o}C and at room temperature were annealed in N_2 ambience, both the devices showed the overall enhanced device performance. The higher filed effect mobility and negative shift in threshold voltage were obtained from the TFTs with IGZO film deposited at the high temperature. It can be concluded that the depositing the IGZO films on a heated substrate effectively enhances the quality of interface between the gate dielectric layer and the IGZO channel layer, resulting in better device performance.

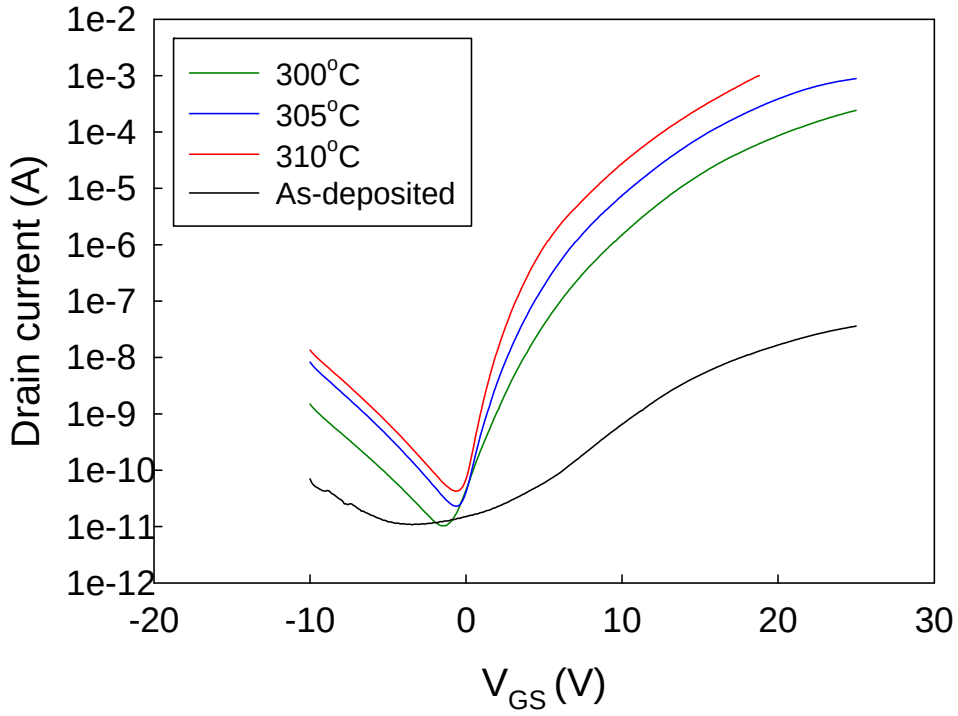

Fig.1.1. Transfer characteristics of RT-TFTs annealed under various temperature for 35min. W/L=200/5, V_{DS}=20V.

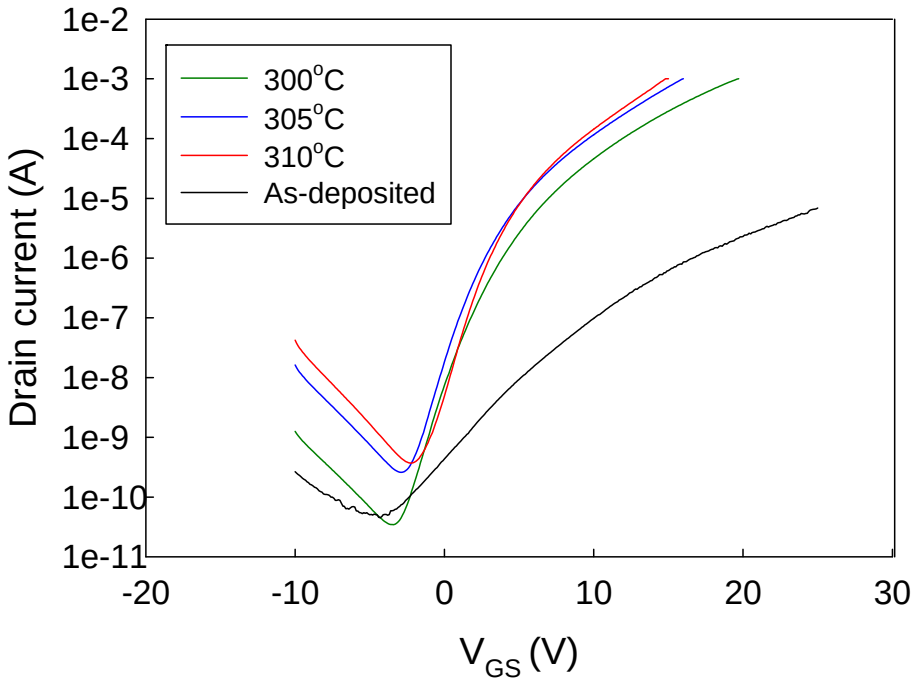

Fig.1.2. Transfer characteristics of HT-TFTs annealed under various temperatures for 35min. W/L=200/5, V_{DS}=20V.

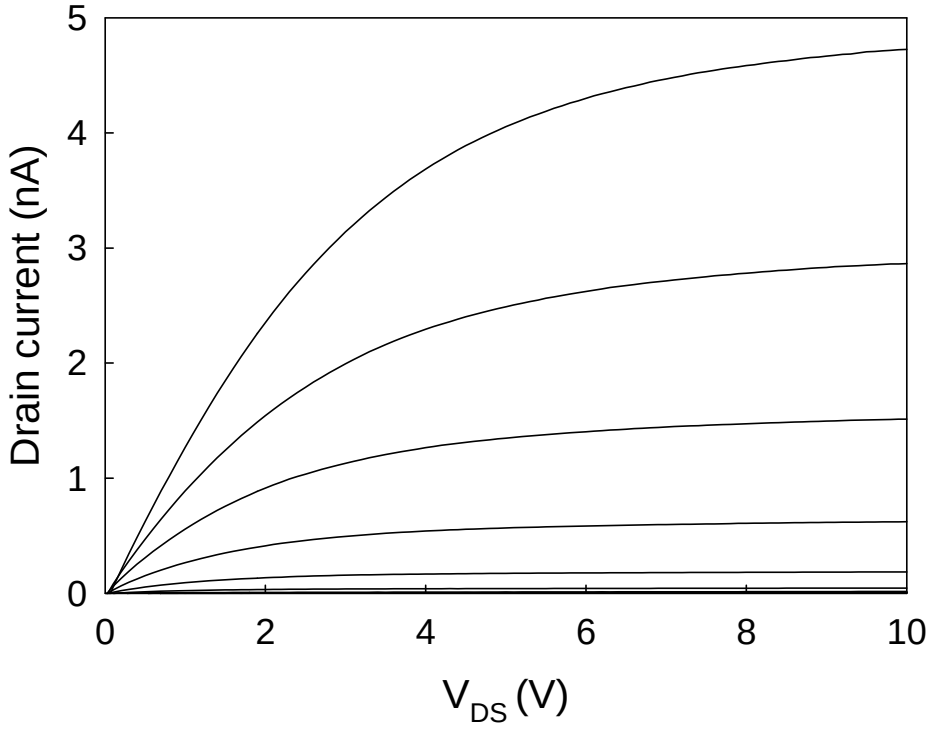

Fig.1.3. Output characteristics of as-deposited RT-TFTs. (V_{GS}=20V, Step:-2V).

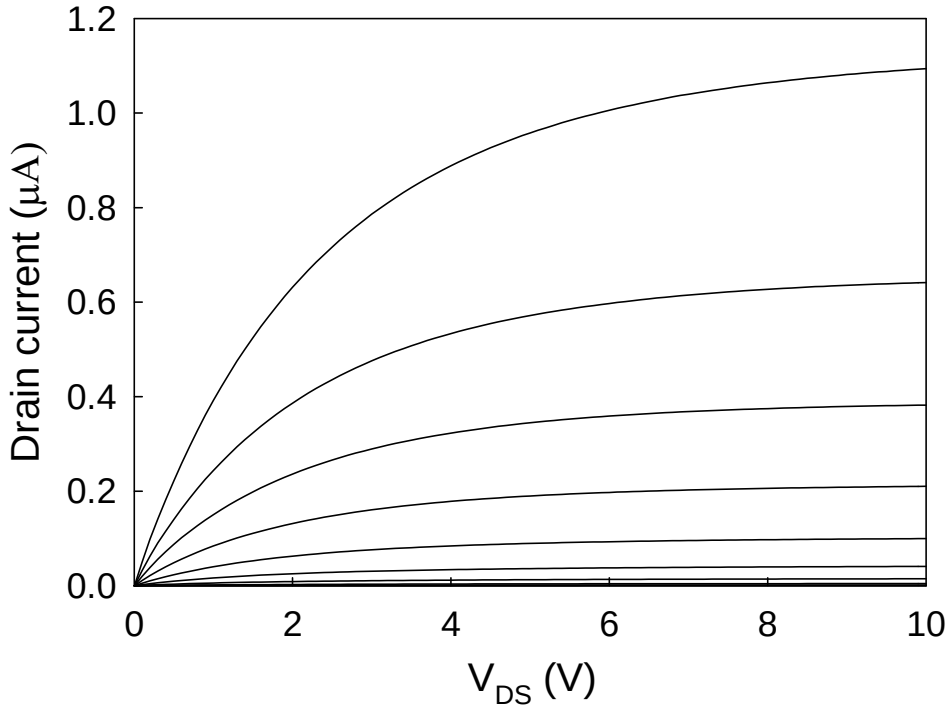

Fig.1.4. Output characteristics of as-deposited HT-TFTs. (V_{GS}=20V, Step:-2V).

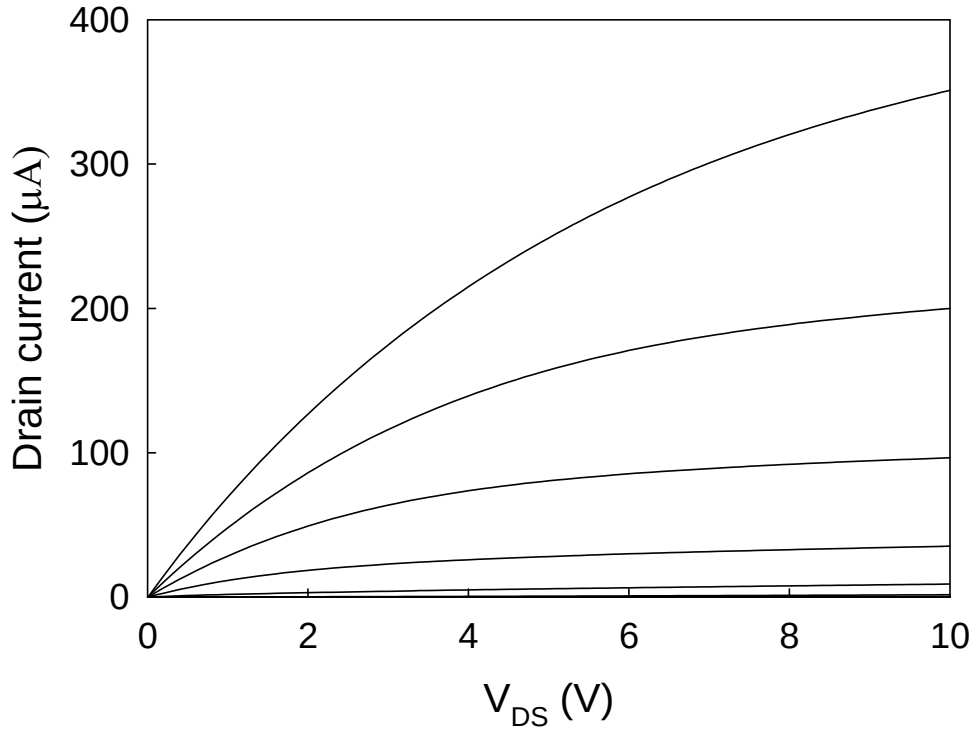

Fig.1.5. Output characteristics of RT-TFTs annealed at 310°C for 35min. (V_{GS}=16V, Step:-2V).

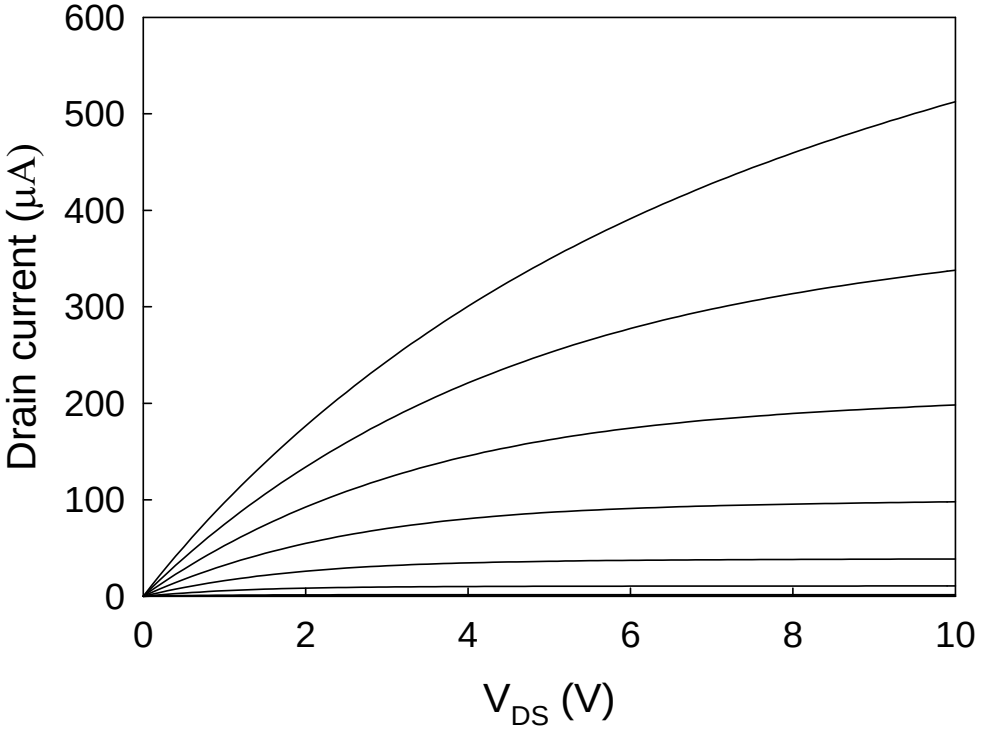

Fig.1.6. Output characteristics of HT-TFTs annealed at 310°C for 35min. (V_{GS}=16V, Step:-2V).

Table.1.1. Summary of the device characteristics of a- IGZO RT-TFTs and HT-TFTs.

	Substrate temperature (^{o}C)							
	Room temperature				200			
Post-annealing condition (^{o}C)	As-deposit	300	305	310	As-deposit	300	305	310
μ_{sat} (cm^2/Vs)	0.001	0.8	2.8	11.0	0.05	6.0	11.0	17.0
V_{th} (V)	8.0	2.8	2.7	1.7	3.1	-0.2	-0.5	-0.1
On-off current ratio	3.3×10^3	2.4×10^7	3.9×10^7	2.4×10^7	2.3×10^5	2.9×10^7	3.9×10^6	2.7×10^6
S (V/decade)	4.60	1.23	0.83	0.73	4.48	1.00	1.04	1.02

Chapter 2.

Hydrogenation of a-IGZO channel layer in the thin film transistors

Introduction

Amorphous indium-gallium-zinc oxide thin-film transistors (a-IGZO TFTs) have been investigated for switching devices in the active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diode (AMOLEDs) displays in recent years. To improve the electrical performance of a-IGZO TFTs, post annealing process has usually been employed. Although rapid thermal annealing (RTA) in N_2 ambiance has conventionally been utilized, the annealing in hydrogen ambiance has also been investigated because hydrogen in ZnO semiconductors was known to act as n-type donor. More recently, a-IGZO TFTs were fabricated by using RF sputtering with Ar/H_2 gas mixture. It was found that the introduction of hydrogen into a-IGZO film effectively passivated interface traps at the interface between the a-IGZO and gate dielectric layer. In this study, we have investigated high pressure hydrogen annealing (HPHA) process to improve the electrical performance of a-IGZO TFTs by introducing hydrogen into the channel material more effectively. For the comparative study, a-IGZO TFTs annealed in N_2 ambiance was also fabricated and their electrical performances were compared with those annealed in high pressure hydrogen ambiance.

Fabrication details of bottom gated a-IGZO TFTs

The fabrication process began with Corning 1737 glass substrates coated with 200-nm-thick indium tin oxide (ITO) (sheet resistance =4~8 Ω/□, Delta Technologies limited, USA). The ITO layer was patterned using photolithography and LCE-12k (ITO etchant, Cyantek Corporation) wet etchant at 33^{o}C for 10min to define bottom gate electrodes. The 50-nm-thick silicon nitride gate insulator was deposited by plasma enhanced vapor deposition system utilizing SiH_4, NH_3, N_2, and He gases at

300^{o}C. After the deposition of silicon nitride, 50-nm-thick undoped IGZO film was grown by rf magnetron sputtering system with facing target configuration. The IGZO films were deposited on a substrate at room temperature (RT-TFTs) and 200^{o}C (HT-TFTs). All the other process parameters were maintained same for the two types of devices. The sputtering conditions were a pure Ar (8sccm), an rf power of 350 W, and working pressure of 5 mTorr. The deposited IGZO film was subsequently patterned by photolithography and a wet etching by diluted HCl (300:1). Silicon nitride gate dielectric was etched by inductively coupled plasma etcher system using SF_6/O_2 gas mixtures to form via holes for contact to ITO gate electrodes. Finally, Multilayer Ti/Pt/Au metallization was e-beam evaporated and lifted-off for source and drain contacts.

After the fabrication, high pressure hydrogen annealing was carried out by controlling hydrogen gas pressure from 1 to 15 atm at 250^{o}C for 20 min. For the control devices, rapid thermal annealing process in N_2 ambiance was applied to the as-deposited TFTs at 300^{o}C for 10, 15, and 20 min.

The electrical characteristics of fabricated TFTs having a channel width (W) of 100 μm and a length (L) of 10 μm were measured using a semiconductor parameter analyzer (HP-4155A).

Results

The electrical characteristics of the as-fabricated devices include the field effect mobility of 0.01 cm^2/Vs, subthreshold slope of 2.31 V/decade, and on/off current ratio of 1.42×10^5.

The transfer characteristics graph of the TFTs treated high pressure hydrogen annealing (HPHA) and TFTs annealed in N_2 ambience processed under various post-annealing condition are shown in Fig.1 and Fig.2, respectively. The transfer characteristics of the devices were measured at V_{DS}=20 V. Table.1. shows the summary of the device characteristics of both TFTs annealed in H_2 ambient and TFTs annealed in N_2 ambient. The device parameters were extracted from the transfer curves of Fig.2.1 and Fig.2.2. Table 2.1. shows that both the post-annealing process improved the performance of the TFTs significantly when they are compared with those of the as-fabricated devices. For the N_2-

annealed devices, the best performances were obtained from the devices annealed for 15min. These devices exhibited the subthreshold slope of 1.22 V/decade, the field-effect mobility of 1.03 cm^2/Vs, and the on/off current ratio of 1.87×10^8. Meanwhile, we have found that the performance of the devices annealed in hydrogen ambiance strongly dependent upon the hydrogen gas pressure. The field effect mobility increased with the hydrogen pressure. The maximum field effect mobility of 10.33 cm^2/Vs was obtained from the devices annealed at 15 atm. However the best on/off current ratio and the lowest subthreshold slope were obtained from the devices annealed at 5 atm. When the devices were annealed at hydrogen pressure of 10 atm, the carrier density increased a lot, but the field effect mobility didn't change much. For the devices annealed under the hydrogen pressure of 15 atm, the current density didn't change much, but the field effect mobility was improved around two times when the device performances are compared with those annealed at the hydrogen pressure of 10 atm.

Fig.2.3 and Fig.2.4 show the output characteristics of IGZO TFTs annealed in hydrogen pressure of 15 atm and IGZO TFTs N_2- annealed at 300^oC for 15min, respectively. A saturation current of TFTs annealed in high pressure H_2 ambience was near 800 μA under a gate bias of 20V, which was significantly higher than that of TFTs annealed in N_2 ambience.

Conclusion

It can be concluded that the hydrogen incorporated in the IGZO channel material effectively increased the carrier concentration leading to the increased current density. When the devices were annealed under the higher hydrogen pressure such as 15 atm, the hydrogen in the IGZO channel effectively passivated the defects in the material so that the field effect mobility was dramatically improved. In summary, by introducing hydrogen in the annealing process, the field effect mobility was improved order of magnitude improved when it is compared with that of the devices annealed in N_2 ambiance.

Table.2.1. Comparison of parameters of device characteristics of a-IGZO TFTs.

	μ_{sat} (cm^2/Vs)	V_{th} (V)	On/Off current ratio	S (V/decade)
As-deposited	0.01	12.11	1.42×10^5	2.31
Annealed in N_2	1.03	11.09	1.87×10^8	1.22
Annealed in H_2, 1 atm	4.90	11.18	5.70×10^5	1.51
Annealed in H_2, 5 atm	5.91	10.27	4.85×10^6	1.27
Annealed in H_2, 10 atm	6.74	8.91	8.7710^5	2.07
Annealed in H_2, 15 atm	10.33	8.98	$2.71 X 10^5$	2.48

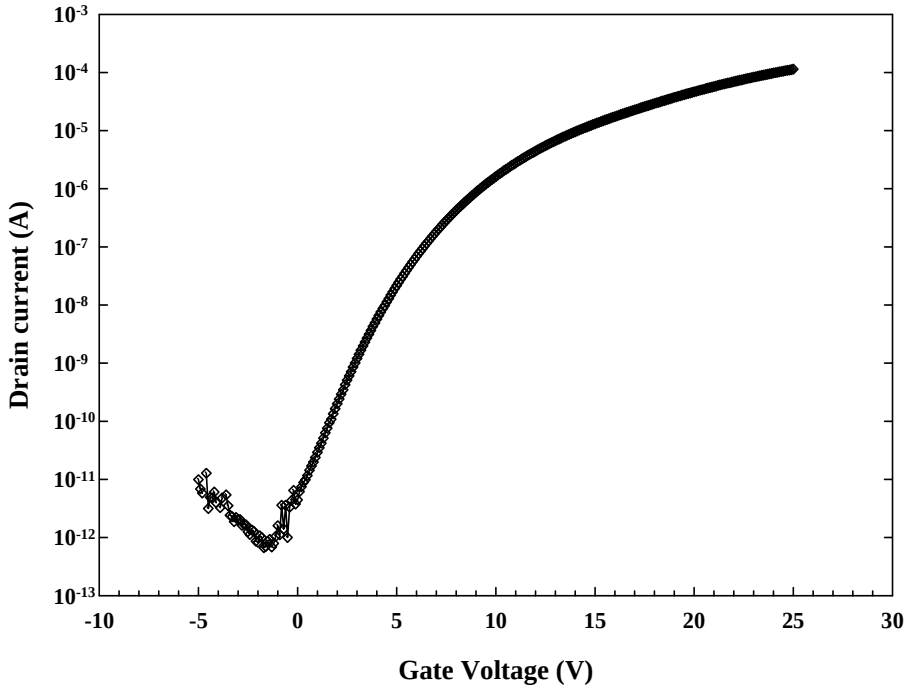

Fig.2.1. Transfer characteristics graphs of fabricated a-IGZO TFTs annealed at 300°C for 15min. (W/L =100µm/10µm, V_{DS}=20V)

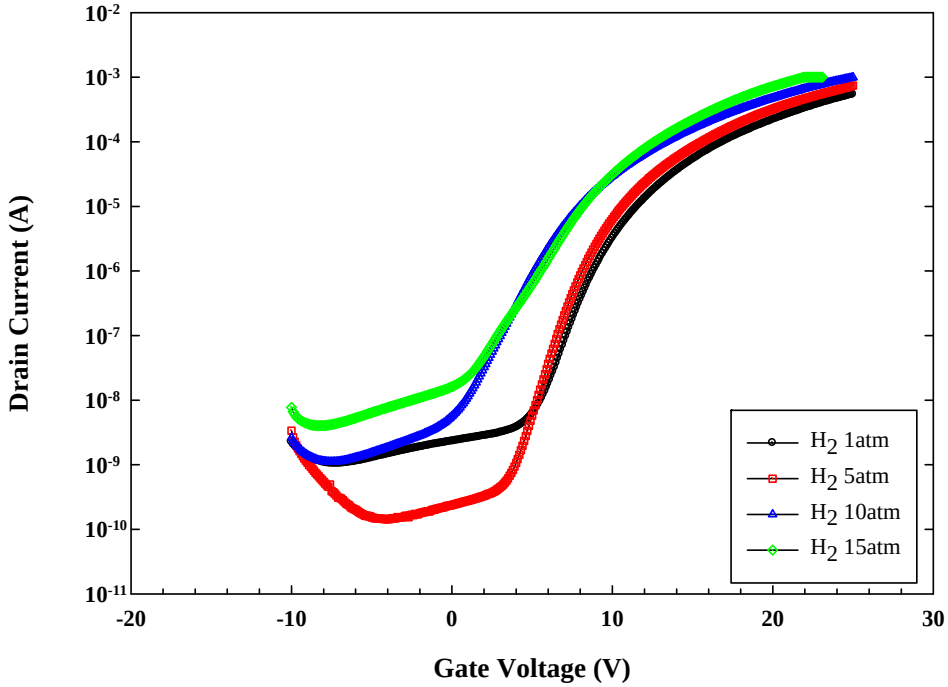

Fig.2.2. Transfer characteristics graphs of a-IGZO TFTs annealed HPHA with H_2 1 atm, 5 atm, 10 atm, and 15 atm. (W/L=100μm/10μm, V_{DS}=20V).

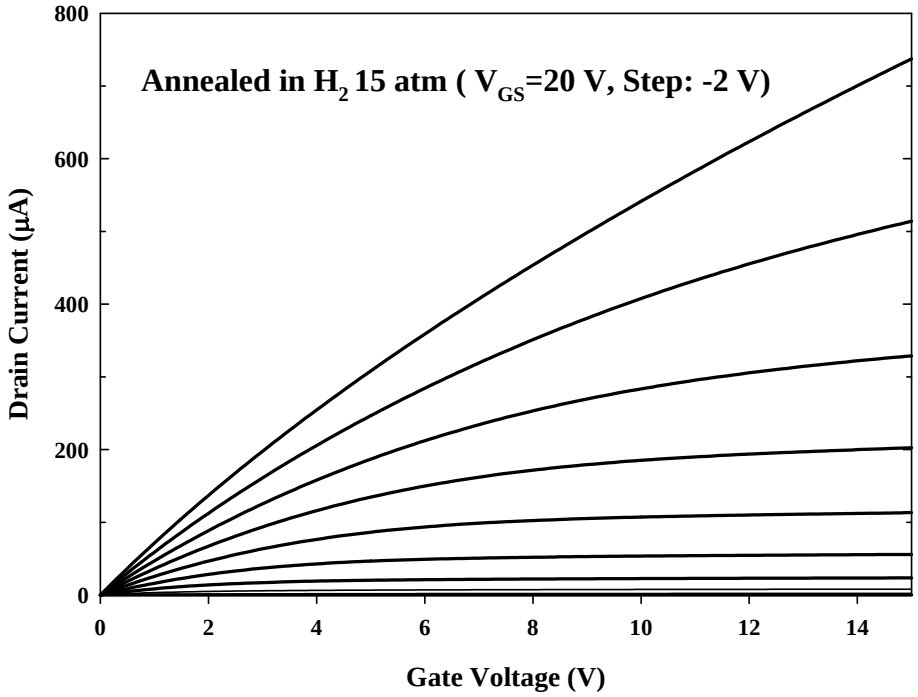

Fig.2.3. Output characteristics of a-IGZO TFT annealed in H_2 pressure of 15 atm. (V_{GS}=20V, Step:-2V).

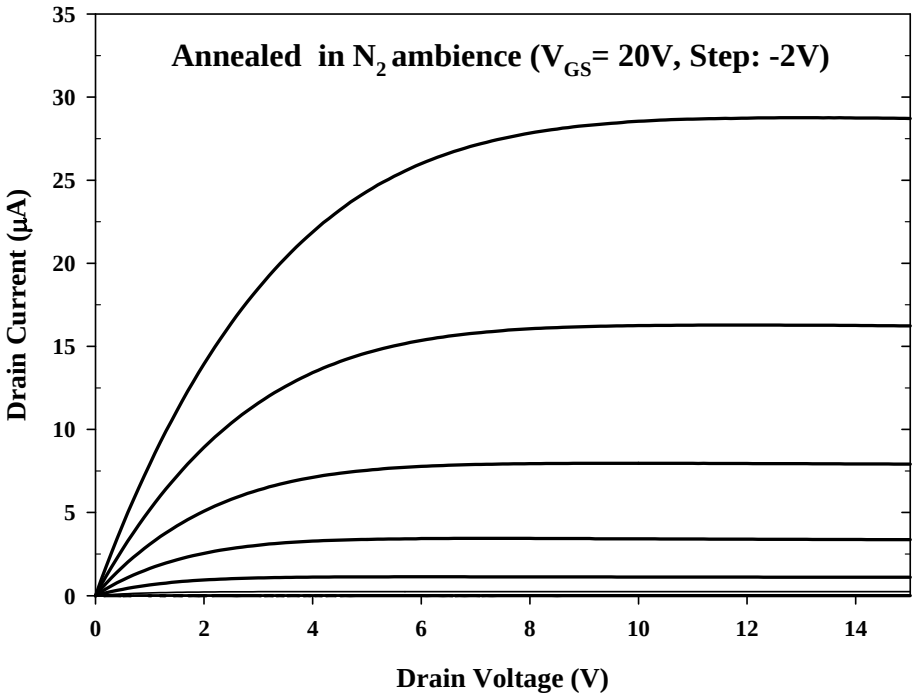

Fig.2.4. Output characteristics of a-IGZO TFT annealed in N_2 ambience. (V_{GS}=20V, Step:-2V).